



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

#1620h
10/29/03

Serial No.: 09/330,231
Applicant: Roberto Passerone, James A. Rowson, Alberto Sangiovanni-Vincentelli
Assignee: **Cadence Design Systems, Inc.**
Filing Date: June 10, 1999
Title: SYSTEM AND METHOD FOR AUTOMATICALLY SYNTHESIZING
INTERFACES BETWEEN INCOMPATIBLE PROTOCOLS

Examiner: Justin King
Group Art Unit: 2181

Attorney Docket No.: 248/248 (7010602001)

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APPEAL BRIEF UNDER 37 CFR § 1.192

The Applicants submit this Appeal Brief pursuant to the Notice of Appeal filed in this case on August 21, 2003. This brief is submitted in triplicate.

I. Real Party in Interest

The real party in interest is **Cadence Design Systems, Inc.** of San Jose, California and is the assignee of this application.

II. Related Appeals and Interferences

No related appeals, nor interferences, are currently pending.

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III. Status of the Claims

Claims 1-22 stand rejected under 35 U.S.C. Section 103. Claims 1-22 are pending.

Claims 1-22 are appealed.

IV. Status of Amendments After Final Rejection

An amendment was filed on June 22, 2003, which was subsequent to the final rejection.

This amendment has been entered.

V. Summary of the Invention

The present invention is defined by claim 1 and its equivalents. The present section of the Appeal Brief is set forth merely to comply with the requirements of 37 C.F.R. Section 1.192(c)(5) and is not intended to limit claim 1 in any way. See MPEP 1206.

A method for exchanging data messages between a first block having a first protocol for exchanging messages and a second block having a second protocol for exchanging messages is performed. A first representation, representing the first protocol, said first representation using regular expressions is received, and a second representation, representing the second protocol, said second representation using regular expressions is received, as shown in Figure 2, element 202, and as discussed on page 10 of the application. A first finite automaton for said first representation is generated, and a second finite automaton for said second representation is generated, as shown in element 204 of Figure 2, the flow chart of Figure 3 and as discussed on pages 21-22 of the specification. The method performs automatically synthesizing an interface between the first and second protocols based on the first and second finite automatons, as shown in Figure 2, elements 206, 208, and as discussed on pages 10-12, 21, and 28.

VI. Issues

The issues presented for appeal are

- (A) whether the examiner can establish a prima facie rejection of claim 1 under 35 U.S.C. Section 103 using a per se rule of obviousness.
- (B) whether a rejection of claim 1 under 35 U.S.C. Section 103 must be based on facts taught by the prior art.
- (C) whether an element of claim 1, which is unknown but for applicant's disclosure, makes the claim nonobvious.
- (D) whether modifying the prior art to produce the invention of claim 1 must be taught by the prior art.
- (E) whether modifying the prior art to produce the invention of claim 1, without showing any teaching in the prior art of such a modification, is impermissible hindsight.

VII. Grouping of claims.

Claims 1-22 stand or fall together and claim 1 is the representative claim.

VIII. Arguments

Claim 1 recites “automatically synthesizing an interface between the first and second protocols based on the first and second automatons.” The examiner rejected claim 1 based on a reference written by Akella et al. (“Akella”), that discloses an interface created by a designer who manually enters the intended behavior of the interface in the form of a finite state machine. The reference clearly fails to show “automatically synthesizing an interface between the first and second protocols based on the first and second automatons” as recited in claim 1. The examiner maintains the rejection using a per se rule of obviousness, that “providing a mechanical or automatic means to replace manual activity which has accomplished the same result is unpatentable.” *In re Venner*, 120 USPQ 192 (CCPA 1958).

Applicants submit that the examiner has failed to establish a prima facie rejection of claim 1 under 35 U.S.C. Section 103.

(A) Can the examiner establish a prima facie rejection of claim 1 under 35 U.S.C. Section 103 using a per se rule of obviousness as stated in *Venner*?

Applicants respectfully submit that the answer is no. The Board of Appeals has specifically forbidden the use of the per se rule of obviousness from *Venner* two times.

The Board of Appeals has said that:

In *Venner*, however, all limitations in the claims, including the automatic means, were disclosed in the applied references.... In the present case, unlike *Venner*, the examiner has not provided a reference which discloses [the claimed automatic element]. The examiner has merely relied on a per se rule that providing a mechanical or automatic means to replace manual activity which has accomplished the same result is unpatentable. As stated

by the Federal Circuit [in *Ochiai*], "reliance upon per se rules of obviousness is legally incorrect and must cease."

In re Brouillet, Appeal No. 1998-2297. The Board has also said that:

The claimed [element] is disclosed as an automatic means. We do not agree with the Examiner that *In re Venner* makes converting any manual operation to an automatic operation routine in the art. There must be some evidence to show the simplicity of converting a particular operation. The mere allegation that it can be done is not convincing.

Ex parte Carlsen, Appeal No. 1997-0402.

(B) Must a rejection of claim 1 under 35 U.S.C. Section 103 be based on facts taught by the prior art?

Applicants submit that a rejection under section 103 must be based on facts taught by the prior art, as stated by the Federal Circuit:

Section 103 requires a fact-intensive comparison of the claimed process with the prior art, rather than the mechanical application of one or another *per se* rule. The use of *per se* rules, while undoubtedly less laborious than a searching comparison of the claimed invention--including all its limitations-- with the teachings of the prior art, flouts section 103 and the fundamental case law applying it. *Per se* rules that eliminate the need for fact-specific analysis of claims and prior art may be administratively convenient for PTO examiners and the Board. But reliance on *per se* rules of obviousness is legally incorrect and must cease. Any such administrative convenience is simply inconsistent with section 103, which, according to *Graham* and its progeny, entitles an applicant to issuance of an otherwise proper patent unless the PTO establishes that the invention *as claimed* in the application is obvious over cited prior art, based on the specific comparison of that prior art with claim limitations. We once again hold today that our precedents do not establish any *per se* rules of obviousness.

In re Ochiai, 71 F.3d. 1565 (Fed. Cir. 1995).

Applicants submit that the examiner incorrectly drew from *Venner*, a case turning on specific facts, a general obviousness rule: namely, that a claim for an automated process is obvious if the prior art references disclose a similar process that is not automated, and applied this rule to claim 1 of the application. However, no such *per se* rule exists. Mere citation of *Venner* or any other case as a basis for rejecting process claims that differ from the prior art by their automated elements is improper, as it sidesteps the fact-intensive inquiry mandated by section 103. In other words, there are not *Venner* obviousness rejections, but rather only section 103 obviousness rejections. See *Ochiai*.

(C) Does an element of claim 1, which is unknown but for applicant's disclosure, make the claim nonobvious?

Applicants submit that if a claimed element is unknown but for applicant's disclosure, then the claim is nonobvious. In other words, it would not have been obvious to those of ordinary skill in the art to choose automatically synthesizing the interface between the first and second protocols as recited in claim 1 because automatically synthesizing the interface is unknown but for Applicant's disclosure. As the Federal Circuit had occasion to observe, "one cannot choose from the unknown." *Ochiai*.

(D) Must modifying the prior art to produce the invention of claim 1 be taught by the prior art?

Applicants submit that modifying the prior art to include the claimed element is obvious only if the prior art teaches the modification. The mere possibility that one of the prior art methods could be modified such that it would lead to automatically synthesizing the interface

recited in claim 1 does not make the process recited in claim 1 obvious "unless the prior art suggested the desirability of [such a] modification." *In re Gordon*, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed.Cir.1984).

The prior art cited by the Examiner fails to suggest any motivation for, or desirability of, changing the prior art to automatically synthesize the interface, as espoused by the Examiner. See *In re Fritch*, 972 F.2d 1260 (Fed. Cir. 1992).

(E) Is modifying the prior art to produce the invention of claim 1 without showing any teaching in the prior art of such a modification impermissible hindsight?

Applicants submit that modifying the prior art without relying on a teaching or suggestion from the prior art is impermissible hindsight. The examiner erred by indulging in an essentially hindsight comparison of "automatically synthesizing the interface" as recited in claim 1 with that of other processes in the prior art that produced other interfaces without automatically synthesizing them. Such a comparison uses Applicant's specification as though it were prior art in order to make the claim to a method that uses the nonobvious automatically synthesizing to make the nonobvious process appear to be obvious. See *Ochiai* and *Fritch*.

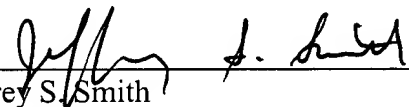
Therefore, applicants submit that claim 1 is patentable under 35 U.S.C. Section 103 over Akella in view of a *Venner* per se rule of obviousness.

IX. CONCLUSION

For the above reasons, Applicants respectfully submit that the rejection of claims 1-22 based on 35 U.S.C. § 103(a) has been overcome. Accordingly, Applicants request that the Board of Patent Appeals and Interferences overrule the Examiner and allow claims 1-22.

DATE: October 15, 2003

Respectfully submitted,

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APPENDIX: Pending Claims

Listing of appealed claims 1-22:

1. A method for exchanging data messages between a first block having a first protocol for exchanging messages and a second block having a second protocol for exchanging messages, the method comprising:

receiving a first representation, representing the first protocol, said first representation using regular expressions;

receiving a second representation, representing the second protocol, said second representation using regular expressions;

generating a first finite automaton for said first representation;

generating a second finite automaton for said second representation; and

automatically synthesizing an interface between the first and second protocols based on the first and second finite automatons.

2. The method of claim 1, further comprising:

automatically corresponding data from said first and second protocols.

3. The method of claim 2, further comprising:

automatically translating data between said first protocol and said second protocol, said data in said first protocol having a first sequence, said data in said second protocol having a second sequence that is different from said first sequence.

4. The method of claim 2, wherein said generating a first finite automaton comprises:

identifying the initial state of the first protocol;
identifying a first sequence of data according to the first protocol;
constructing derivatives of regular expressions; and
eliminating equivalent expressions.

5. The method of claim 4, wherein said identifying a first sequence of data comprises:
collecting data that is transferred during one or more transitions; and
integrating said data with previous transitions.
6. The method of claim 5, further comprising:
automatically translating data between said first protocol to said second protocol,
said data in said first protocol having the first sequence, said data in said second protocol
having a second sequence that is different from said first sequence.
7. The method of claim 1, further comprising:
automatically translating data between said first protocol to said second protocol,
said data in said first protocol having a first sequence, said data in said second protocol
having a second sequence that is different from said first sequence.
8. The method of claim 21, wherein automatically generating a third representation
comprises:
(a) selecting the interface state representing a first finite automaton state and a
second finite automaton state;

- (b) identifying all outgoing transitions in said selected state;
 - (c) determining a new state for each outgoing transition;
 - (d) repeating steps (a)-(c) for each interface state.
9. The method of claim 8, wherein generating a third representation comprises:
- identifying said permitted operations as operations that do not result in a data inconsistency.
10. The method of claim 8, wherein said eliminating comprises:
- identifying non-deterministic transitions for each interface state;
 - selecting a single outgoing transition for each interface state for each input value based upon priority parameters to generate a deterministic interface between the first and second protocols.
11. The method of claim 1, wherein said generating a first finite automaton comprises:
- identifying the initial state of the first protocol;
 - identifying a first sequence of data according to the first protocol;
 - constructing derivatives of regular expressions; and
 - eliminating equivalent expressions.
12. A computer based system for exchanging data messages between a first block having a first protocol for exchanging messages and a second block having a second protocol for exchanging messages, the system comprising:

storage device to store data and sequences of operations;

a processor to receive signals from said storage device and to execute said sequences of operations;

a receiving unit to transmit signals to said processor and to receive a first and second representation, representing of the first and second protocols, said first and second representations using regular expressions;

an automata unit to generate a first finite automaton for said first representation and to generate a second finite automaton for said second representation; and

a synthesizing unit to automatically synthesize an interface between the first and second protocols based on the first and second finite automata.

13. The system of claim 12, further comprising:

a corresponding unit to receive signals from said processor and to automatically correspond data from said first and said second protocol.

14. The system of claim 13, further comprising:

a translation unit to automatically translate data between said first protocol and said second protocol, said data in said first protocol having a first sequence, said data in said second protocol having a second sequence that is different from said first sequence.

15. The system of claim 13, wherein said automata unit comprises:

a first identifying unit to identify the initial state of the first protocol;

a second identifying unit to identify a first sequence of data according to the first protocol;

a derivative unit to construct derivatives of regular expressions; and
an eliminating unit to eliminate equivalent expressions.

16. The system of claim 15, wherein said second identifying unit comprises:

a data collection unit to collect data that is transferred as one or more transitions;
and
a data analyzer to integrate said data with previous transitions.

17. The system of claim 12, further comprising:

a translation unit to automatically translate data between said first protocol and
said second protocol, said data in said first protocol having a first sequence, said data in
said second protocol having a second sequence that is different from said first sequence.

18. The system of claim 12, wherein the product unit comprises:

a selection unit to select an interface state representing a first finite automaton
state and a second finite automaton state;
an identifying unit to identify outgoing transitions in said selected state;
a state unit to determine a new state for each outgoing transition;

19. The system of claim 18, wherein the product unit further comprises:

a consistency unit to identify said permitted operations as operations that do not
result in a data inconsistency.

20. A computer readable medium storing instructions which, when executed by a processing system, cause the system to perform a method for exchanging data messages between a first block having a first protocol for exchanging messages and a second block having a second protocol for exchanging messages, the method comprising:

- receiving a first representation of the first protocol;
- receiving a second representation of the second protocol;
- generating a first finite automaton for said first representation;
- generating a second finite automaton for said second representation;
- generating a third representation of one or more permitted operations of said first and second finite automata; and
- automatically eliminating non-determinisms in said third representation.

21. The method of claim 1, further comprising:

- automatically generating third representation, representing one or more permitted operations of said first and second finite automata.

22. A method for exchanging data messages between a first block having a first protocol and a second block having a second protocol, the method comprising:

- generating a first finite automaton corresponding to the first protocol;
- generating a second finite automaton corresponding to the second protocol;
- generating a representation of one or more permitted operations of the first and second finite automata; and
- automatically eliminating at least one non-determinism in the representation.